

END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE 2018

Paper Code: BCA106

Subject: Digital Electronics

Time : 3 Hours

Maximum Marks :75

Note: Attempt any five questions including Q.no.1 which is compulsory.
Select one question from each unit.

- Q.1 Attempt all the questions:- (5x5=25)
- (a) Why are NAND and NOR gates known as universal gates? Implement half adder circuit using NAND gates only.
 - (b) Define the terms for digital circuits:
 - (i) Speed of operations, (ii) Figure of Merit (iii) Noise margin.
 - (c) What is De-multiplexer? Explain the difference between MUX and DEMUX.
 - (d) What is the major disadvantage of SR flip-flop? How is this addressed in JK Flip-Flop?
 - (e) Explain ripple counter. What's the difference between ripple counter and synchronous counter?

Unit-I

- Q.2 (a) Explain deMorgan's theorem. Prove the following using De Morgan's theorem: 8.5
- (i) $AB + CD = \overline{\overline{AB} \cdot \overline{CD}}$ and (ii) $(A + B) \cdot (C + D) = \overline{\overline{(A + B)} + \overline{(C + D)}}$
- (b) Implement EX-OR and EX-NOR gate using only NOR gates 4
- Q.3 (a) Explain the term "logic family". Compare RTL and TTL logic. 3
- (b) Simplify the following expression using K-map: 5
- $Y = m_0 + m_1 + m_3 + m_7 + m_8 + m_9 + m_{11} + m_{15}$
- (c) Prove the relationship:
- (i) $\overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C} + A \cdot B \cdot C = A \cdot B + B \cdot C + C \cdot A$ 3
- (ii) $A \cdot \overline{B} + A \cdot B + B \cdot C = A + B \cdot C$ 1.5

UNIT-II

- Q.4 (a) Explain even parity and odd parity. Design a circuit for even parity generator for 3-bit message. 5.5
- (b) Show block diagram of a 3 bit parallel binary adder. 3
- (c) Explain the binary multiplication method using the example (1010x1011) 4
- Q.5 (a) Implement the expression using a multiplexer 6.5
- $f(A, B, C, D) = \sum m(0, 2, 3, 6, 8, 9, 12, 14)$
- (b) Design a 3:8 decoder using basic logic gates. 6

Unit III

- Q.6 (a) Design a S-R latch using 2-input NOR gates 3
- (b) Explain (a) J-K Flip-Flop can be converted to T Flip-Flop, (b) race around condition. 7.5
- (c) Explain master-slave flip-flop 2
- Q.7 (a) Justify the statement: "J-K Flip-Flop is a universal Flip-Flop." 5.5
- (b) Explain the advantage of SIPO over SISO. Discuss their applications. 4
- (c) What is Bi-directional Flip-Flop? 3

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Unit-IV

- Q.8 (a) How ripple counter works? 2.5
(b) Show state diagram of 3 bit up/down counter. Design 3 bit up/down counter using T flip-flop. 7.5
(c) Define ring counter 2
- Q.9 Write short notes on any two of the following: (6.25x2=12.5)
(i) RAM & ROM
(ii) PLA
(iii) Modulo counters

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