(Please write your Exam Roll No.) *Exam Roll No. .....*

END TERM EXAMINATION

SECOND SEMESTER [BCA] MAY-JUNE 2019

Paper Code: BCA-106 ***Subject: Digital Electronics***

Time: 3 Hours ***Maximum Marks: 75***

Note: Attempt any five questions including Q.no.1 which is compulsory. Select one questions from each unit. Assume missing data if any.

Q1 Attempt **any five** questions:

(a) Explain Parity Generation and checking process with example. **(4)**

(b) Explain Excess-3, BCD and gray codes. Convert binary 1101 to equivalent gray code and also convert Gray code 0111 to equivalent Binary code. **(4)**

(c) Perform the following conversions: **(3)**

(i) $(A3.1E)_{16} = (\quad)_{10}$

(ii) $(532.03)_8 = (\quad)_{16}$

(d) Define fan-in, fan-out, propagation delay, noise margin and voltage parameters. **(3)**

(e) What is a D flip flop? Show how SR flip flop can be converted to D flip flop? **(3)**

(f) Explain the working of Serial in Serial Out shift right register. **(4)**

(g) What is binary multiplier? Discuss the multiplier using shift method. **(4)**

Unit-I

Q2 (a) Design the circuit of the Boolean Equation: **(4.5)**

$Y = (\overline{A} + \overline{B})(A + \overline{C} + \overline{D})(A + \overline{B} + C)$ B using only NOR GATES.

(b) Why NAND & NOR Gates are called Universal Gates? How an AND Gate can be implemented using only NOR Gates? **(4)**

(c) Implement Ex-OR using NAND gates only. **(4)**

Q3 (a) Simplify the following Boolean Equation using Boolean Algebra Laws: **(4)**

$Y = \overline{AC(ABD)} + \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}$

(b) Simplify the expression **F = Σ_m (0,2,3,6,7) + Σ_d (8,10,11,15)** using the K-Map method. **(4)**

(c) Express the function **Y = A + BC** in both: **(4.5)**

(i) Canonical SOP form

(ii) Canonical POS form

Unit-II

Q4 (a) Design a Full Adder Circuit using two Half Adders. **(4)**

(b) Design a 1:8 DMUX Circuit. How a 16:1 MUX can be designed using two 8:1 MUX and one OR Gate? **(4)**

(c) What is an encoder? Discuss the design of 8:3 (octal to binary) encoder. **(4.5)**

Q5 (a) What are Multiplexers & DeMultiplexers? Implement the following function using Multiplexer. **(6.5)**

F(A,B,C,D) = Σ_m (0,1,2,3,4,6,8,9,13,14)

(b) Design a 4-bit Parallel Adder/Subtractor with controlled inverter and explain its working. **(6)**

P.T.O.

P1

Unit-III

Q6 (a) Differentiate between Combinational and Sequential circuit. Design a S-R latch using 2 input NOR gates. **(6)**

(b) What is Race-Around Condition and how it can be eliminated in Master-Slave JK Flip Flop? **(6.5)**

Q7 (a) What are Shift Registers? The content of a 4-bit shift register is initially 1101. The register is shifted 4 times to the right with the serial input being 101101. What will be the final content of the register after all the 4 shifts are over? **(6)**

(b) Explain in detail the construction and working of Universal/Bi-Directional shift register. **(6.5)**

Unit-IV

Q8 (a) What is MOD 6 counter? Draw its state diagram and circuit. **(6)**

(b) Draw and Explain the working of ripple counter. **(6.5)**

Q9 (a) Differentiate between RAM and ROM. **(4)**

(b) Explain Johnson counter with truth table and clock pulses. **(4)**

(c) Draw and explain Asynchronous 3 bit up/down counter. **(4.5)**

****